Application Note

NOVOSENSE

Introduction to and Comparative Analysis of Chip-Level ESD and System-Level ESD Test Standards

AN-13-0009

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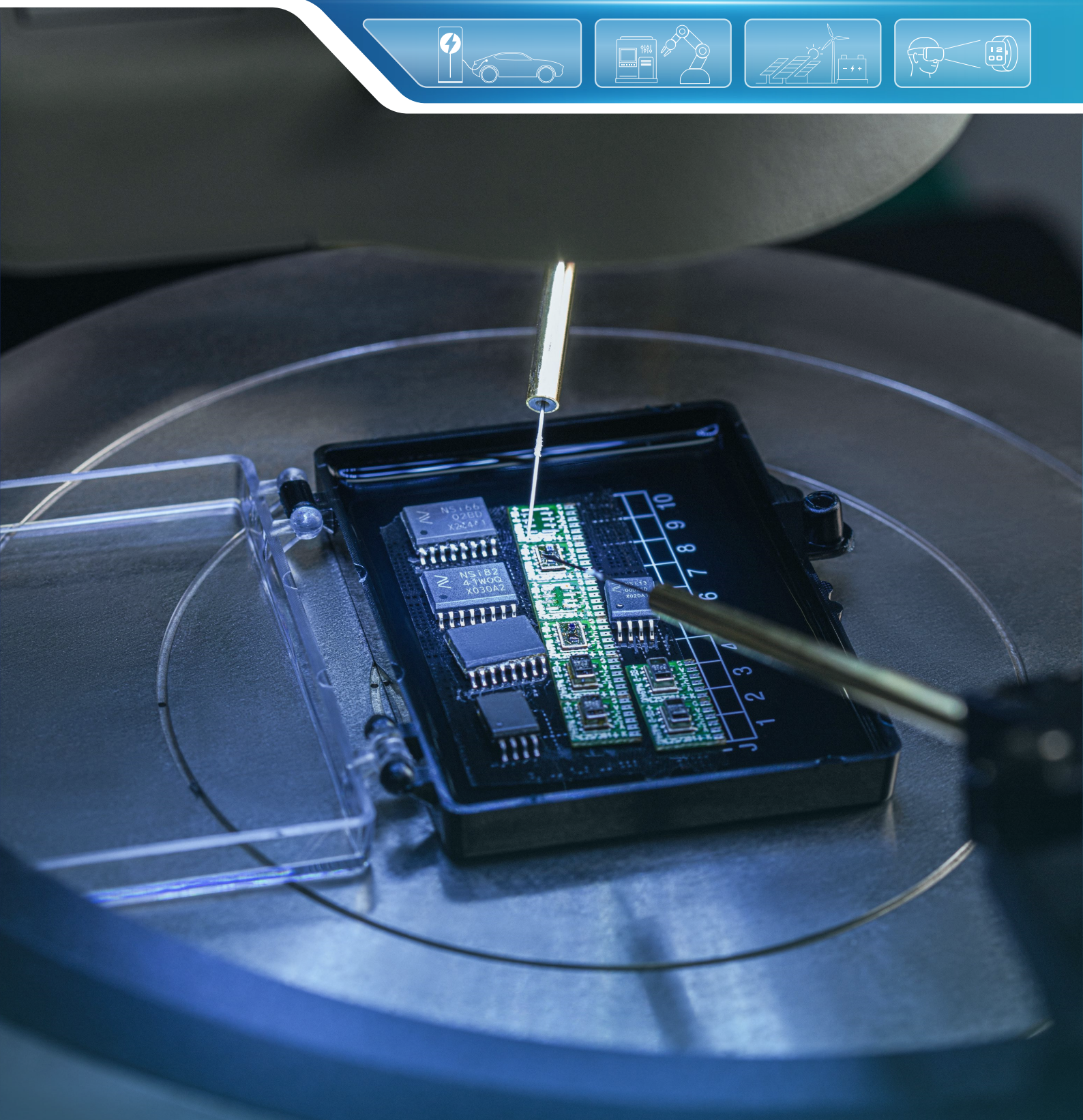

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ABSTRACT

With the continuous scaling down of semiconductor process nodes, electrostatic discharge (ESD) poses a significant challenge to chip reliability. This article introduces the test standards, methods, and levels for chip-level ESD (HBM, CDM, and MM) and system-level ESD (IEC 61000-4-2). It also makes a comparative analysis of chip-level ESD and system-level ESD. Additionally, it discusses commonly used ESD protection design methods for isolation systems and key considerations during testing.

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1.Introduction to ESD

Electrostatic discharge (ESD) refers to the process of charge neutralization between two objects with opposite polarities, which can occur through direct contact or via an electrostatic field. With the widespread adoption of integrated circuits (ICs) and the continuous scaling down of semiconductor process nodes, ESD has become a critical challenge affecting chip reliability. To enhance robustness, modern ICs typically integrate on-chip ESD protection circuits. ESD tests of electronic components have been incorporated as an essential part of electromagnetic compatibility (EMC) testing in both China's national standards and international codes.

Since ESD events may occur throughout the lifecycle of a chip, existing ESD testing standards are categorized into chip-level ESD and system-level ESD. As illustrated in Figure 1.1, chip-level ESD testing primarily evaluates a device's anti-static performance during wafer dicing, packaging, pre-delivery testing, and transportation. In contrast, system-level ESD testing characterizes the chip's immunity to complex electrostatic environments in real-world end-user applications. Due to differences in test methods, chip operating conditions, and test environments, there is generally no direct correlation or comparability between the voltage levels specified in chip-level ESD and system-level ESD testing standards. This article outlines the testing standards for both chip-level ESD and system-level ESD and explores their key differences.

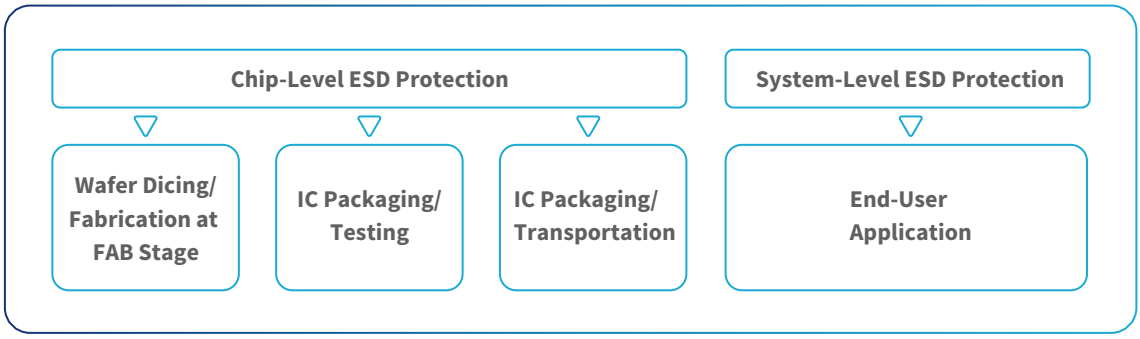


Figure 1.1 Chip-Level ESD vs. System-Level ESD Throughout the IC Lifecycle

2.Chip-Level ESD Testing

2.1.Introduction

Chip-level ESD testing establishes unified criteria for evaluating a chip's ESD resistance during manufacturing, packaging, transportation, and soldering processes. Depending on different electrostatic generation mechanisms and circuit damage modes, chip-level ESD testing primarily includes three models: Human Body Model (HBM), Charged Device Model (CDM), and Machine Model (MM). In industry practice, HBM and CDM are the most widely adopted models for pre-delivery chip testing.

2.1.HBM

The HBM simulates the process where a human body accumulates certain electrostatic charge through friction or other reasons, and the electrostatic charge flows from the human body through the IC pin to ground when the human body contacts the pins of the IC. The widely adopted international standards include JEDEC JS-001 and AEC-Q100-002. In these standards, the charged human body is modeled using a 100 pF capacitor and a 1500 Ω discharge resistor, as shown in Figure 2.1.

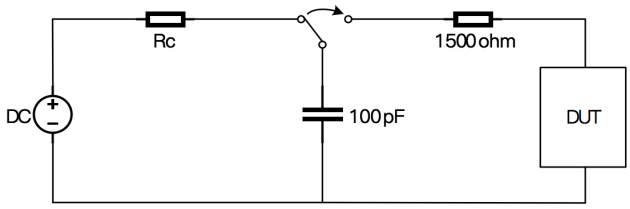


Figure 2.1 Equivalent Circuit Schematic of HBM

Since ESD events are random, any two pins on an IC may experience HBM discharge. Therefore, assessing the ESD resistance of a chip requires testing all possible pin combinations. For HBM testing of a chip, the following combinations of I/O, VDD, and VSS pins are typically adopted (for isolated ICs, I/O corresponds to primary/secondary input/output and Enable pins; VDD corresponds to primary/secondary power supply pins; VSS corresponds to primary/secondary GND pins):

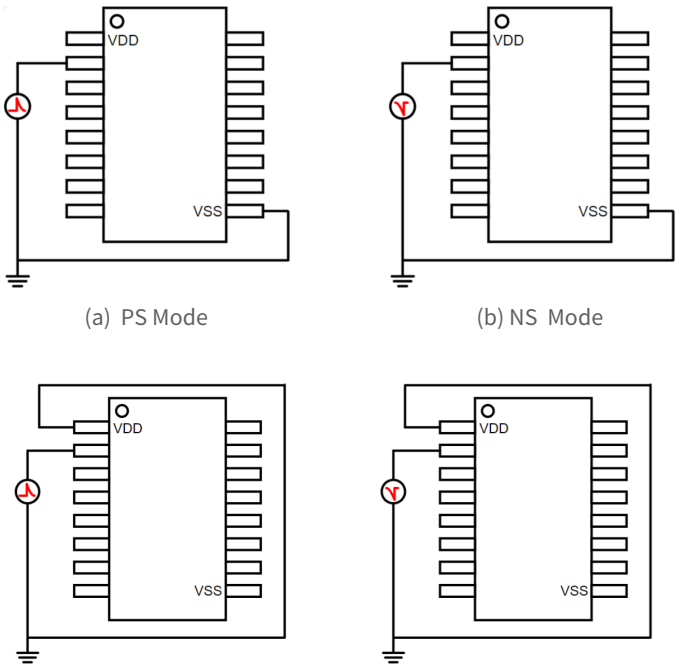
(1) I/O-to-VDD/VSS Discharge Tests

(a) PS Mode: VSS as reference ground; apply positive ESD pulse to I/O pin, with other pins floating.

(b) NS Mode: VSS as reference ground; apply negative ESD pulse to I/O pin, with other pins floating.

(c) PD Mode: VDD as reference ground; apply positive ESD pulse to I/O pin, with other pins floating.

(d) ND Mode: VDD as reference ground; apply negative ESD pulse to I/O pin, with other pins floating.



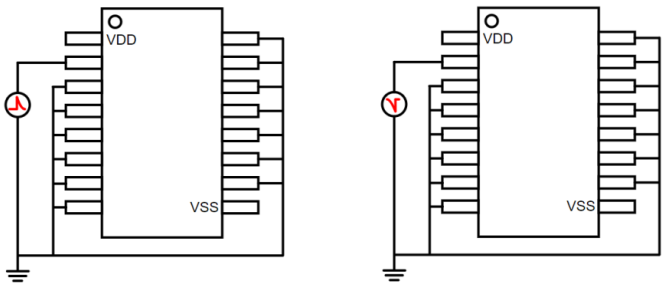
(a) PS Mode (b) NS Mode

(c) PD Mode (d) ND Mode

Figure 2.2 Pin Combinations for IO-to-VDD/VSS Test

(2) I/O-to-I/O Discharge Tests

VDD and VSS pins floating; apply positive and negative ESD pulses to the target I/O pin while shorting other I/O pins to reference ground.

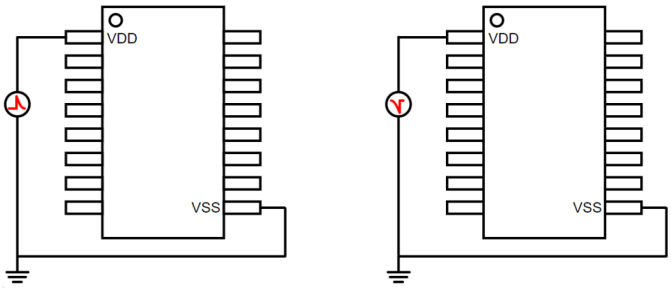


(a) (b)

Figure 2.3 Pin Combinations for IO-to-IO Test

(3) VDD-to-VSS Discharge Tests

VSS as reference ground; apply positive and negative ESD pulses to VDD, with other I/O pins floating.



(a) (b)

Figure 2.4 Pin Combinations for VDD-to-VSS Test

For ICs with multiple power domains, corresponding tests must also be conducted between VDD and VSS and between I/O pins across different power domains.

For each test combination, the chip's test pins are subject to the same ESD voltage three times, with one-second intervals between pulses. Subsequently, whether the tested pin has been damaged by ESD is judged, typically by comparing the measured IV curve of the tested pin and the standard IV curve. A deviation exceeding 30% is considered a failure. If the device does not fail, the ESD voltage is increased, and the above-mentioned test procedure repeated. The adjustment levels for HBM test voltages are listed the table below, where the ESD test voltage causing chip failure is designated as the Electrostatic Discharge Fault Threshold Voltage. The failure criteria will be discussed in detail in subsequent application notes.

Class	Voltage Range (V)	Class	Voltage Range (V)
Class 0Z	0～50	Class 1C	1000～2000
Class 0A	50～125	Class 2	2000～4000
Class 0B	125～250	Class 3A	4000～8000
Class 1A	250～500	Class 3B	⩾8000
Class 1B	500～1000	/	/

Table 2.1 HBM Voltage Levels per JEDEC JS-001

2.2.MM

The Machine Model (MM), also known as the 0-Ω model, simulates the effects on devices when a conductor becomes charged with static electricity. Widely adopted international standards include JESD22-A115-A, AEC-Q100-003, and IEC 61340-3-2S. IC manufacturing is primarily performed using robotic arms. When electrostatic charge from the robotic arms contact the IC pins and form a current path to ground, an instantaneous ESD event occurs. Due to the smaller Ron and larger parasitic capacitance of automated metal machinery, the response time of the ESD pulse generated during this process is shorter. The main differences between MM and HBM include the removal of the 1500 Ω resistor and increasing the capacitance to 200 pF, as shown in Figure 2.5.

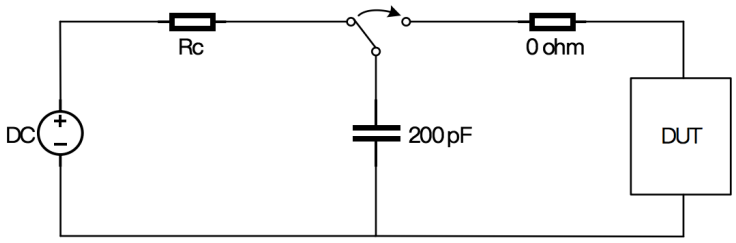


Figure 2.5 Equivalent Circuit Schematic of MM

MM ESD protection levels are classified by ESD stress magnitude, as shown in Table 2.2.

Class	Voltage Range (V)	Class	Voltage Range (V)
M0	0～50	M3	200~400
M1	50～100	M4	400~800
M2	100~200	M5	>800

Table 2.2 MM Voltage Levels per IEC 61340-3-2S

MM shares failure mechanisms with HBM, but exhibits greater test variability due to higher sensitivity to parasitic effects in testing equipment, and lower test reproducibility. Additionally, MM is less stable than CDM in validating metal-to-metal ESD. Therefore, with increasingly stringent control over ESD release from robotic arms in IC manufacturing, the design requirements for MM testing have been gradually de-emphasized. The industry generally relies on HBM and CDM testing to characterize the chip-level ESD robustness.

2.3.CDM

The Charged Device Model (CDM) simulates ESD events caused by charge/discharge of ICs, i.e. the ESD phenomenon resulting from the discharge of accumulated electrostatic charge within the chip. This is fundamentally different from HBM's electrostatic generation mechanism. Key international standards include JEDEC JS-002 and AEC-Q100-011.
The equivalent circuit for CDM is shown in the figure below, with the dashed box representing the equivalent parasitic circuit of the Device Under Test (DUT), and R_{CDM} representing the test current-limiting resistor. Due to significant variations in parasitic resistance, inductance, and capacitance within the chip, which are sensitive to chip type and environmental factors, these parameters are typically not quantified.

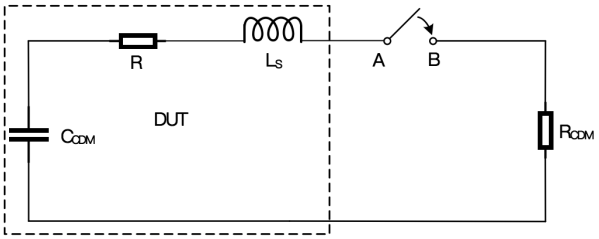
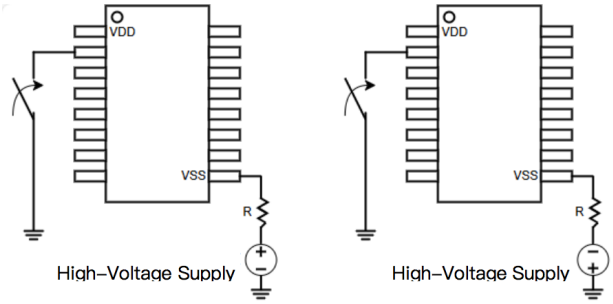


Figure 2.6 Equivalent Circuit Schematic of CDM

Each pin in CDM testing undergoes at least one positive and negative discharge test. Before testing, the chip's VSS pin is connected to a power source to charge it, with both positive and negative charging voltages applied. A current-limiting resistor R (>10 MΩ) is used to prevent excessively high charging voltage from directly damaging the IC. After charging, the power source is disconnected, and other pins of the IC (including I/O and VDD) are respectively grounded for discharge to perform CDM tests, while keeping other non-discharged pins floating.



(a) (b)

Figure 2.7 CDM Test Configuration Diagram

The failure criteria for CDM testing are the same as those for HBM. Testing should start from the lowest voltage level, and after completing a voltage level test, the voltage is progressively increased. The adjustment levels for CDM test voltages are listed in the table below.

Class	Voltage Range (V)	Class	Voltage Range (V)
Class C0a	0~125	Class C2a	500~750
Class C0b	125~250	Class C2b	750~1000
Class C1	250~500	Class C3	⩾1000

Table 2.3 CDM Voltage Levels per JEDEC JS-002

3.System-Level ESD Testing

Chip-level ESD tests, including HBM and CDM, can minimize ESD events during chip manufacturing, packaging, transportation, and soldering processes. However, they cannot accurately simulate the ESD phenomena of chips in real-world end-user applications. System-level ESD testing focuses on simulating ESD impacts in real-world applications, with the widely adopted international standard being IEC 61000-4-2. It's important to note that IEC 61000-4-2 is a general standard for system immunity testing, where the DUT is a fully designed product consisting of PCBs, various ICs, and other functional components interconnected via PCB traces. The ESD stress is shared by all chips along the discharge path. Therefore, using IEC 61000-4-2 to test a single chip does not equivalently represent the chip's true ESD resistance within a system. The ESD discharge circuit specified in IEC 61000-4-2 is shown in the figure below. It uses a 150 pF capacitor to simulate the electrostatic environment and discharges to the DUT through a 330 Ω resistor.

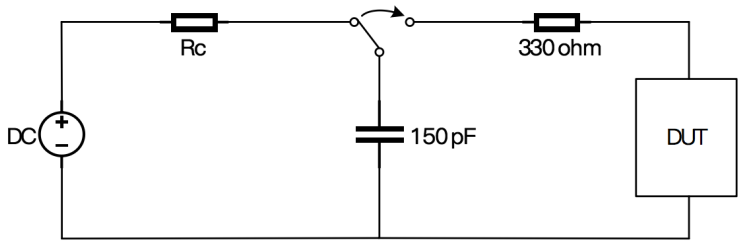


Figure 3.1 Equivalent Circuit Schematic of IEC 61000-4-2 Model

IEC 61000-4-2 defines two testing modes: Contact Discharge and Air Discharge, corresponding to contact levels and air gap levels. In each test mode, at least 10 discharges (with both positive and negative polarities) must be applied to the DUT, with a one-second interval between every two discharges. Testing should start from the lowest voltage level, and after completing a voltage level test, the voltage is progressively increased. The adjustment levels for system-level ESD test voltages are listed in the table below.

Contact Discharge Mode		Air Discharge Mode	
Class	Test Voltage (kV)	Class	Test Voltage (kV)
1	2	1	2
2	4	2	4
3	6	3	6
4	8	4	8
Special(1)	/	Special(1)	/
(1) Open levels, which may be higher or lower than standard ratings, must be defined in the specifications of dedicated equipment. If the voltage exceeds the values listed in the table, specialized testing equipment might be required.			

Table 3.1 System-Level ESD Voltage Levels per IEC 61000-4-2

4.Differences Between Chip-Level and System-Level ESD Testing

Chip-level ESD and system-level ESD tests collectively reflect the ESD performance of a device's ESD robustness throughout its lifecycle, but they differ in test objects and test standards. Chip-level ESD tests use individual ICs as the DUT to evaluate the chip's intrinsic ESD protection. In contrast, system-level ESD tests use complete products as the DUT to assess the entire product's immunity to external ESD events. Consequently, the integrated ESD protection circuits in the chip may not be sufficient to withstand equivalent system-level ESD stresses, which explains why direct system-level ESD testing on chips often leads to failures.

In terms of test methods, chip-level ESD tests are conducted on fixed fixtures with the chip powered off. In contrast, system-level ESD tests involve soldering the chip onto a PCB, where the chip might be powered on during testing, and the pin configurations vary depending on different system circuit connections. Additionally, HBM testing requires three pulses of positive and negative polarity each, while IEC 61000-4-2 requires at least ten pulses of positive and negative polarity each, leading to cumulative charge effects and consequent faster chip damage.

Comparing the discharge pulse waveform parameters, there are significant differences in terms of pulse voltage range, rise time, and number of pulse impacts between chip-level and system-level ESD, as shown in the table below.

Parameter	HBM	CDM	MM	IEC61000-4-2
Voltage Range (V)	0 - ⩾8000	0 - ⩾1000	0 - ⩾800	2000 - 15000
Peak Current (A)	1.3	5	3	30
Rise Time (nS)	25	<1	5	<1
Pulse Count	2	2	2	20

Table 4.1 Waveform Characteristics: Chip-Level ESD vs. System-Level ESD

The differences between the two testing modes can be more intuitively observed in the discharge pulse waveforms, as shown in the figure below.

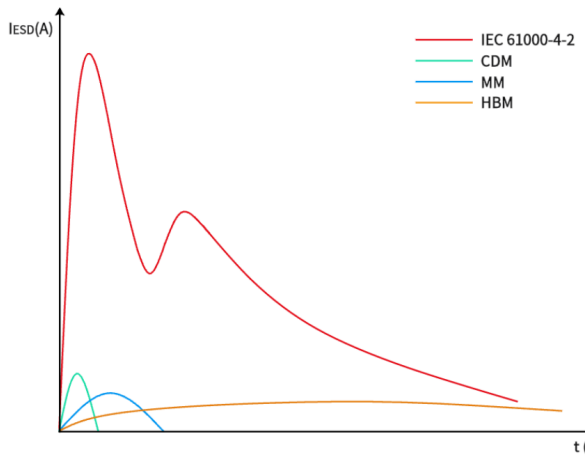


Figure 4.1 Schematic Diagram of Discharge Pulse Waveforms: Chip-Level ESD vs. System-Level ESD

It can be seen that the ESD energy in IEC 61000-4-2 tests is far higher than that of HBM and CDM. Taking 8 kV contact discharge as an example, system-level ESD testing generates a peak current of 30A, compared to 1.3 A for HBM and 5 A for CDM. This implies that system-level ESD imposes six times greater electrical stress on chip's internal protection components relative to chip-level ESD. Moreover, the rise time for system-level ESD pulses ranges from 0.7 ns to 1 ns, compared to the typical rise time requirement of 25 ns in HBM. This stricter response time requirement makes the HBM-optimized protection circuits insufficiently responsive, potentially leading to direct damage to the functional circuits of the chip.

5.System-Level ESD Protection

System-level ESD protection must cover designs from the peripheral circuits of the chip to the entire system, including PCB layout, interface connections, and selection of protective components. In the isolated systems shown in Figure 5.1, particular attention must be paid to the system-level ESD performance of the following two IC categories:

(1) Interface ICs (e.g., CAN, RS-485): These components directly connect to external environments and are vulnerable to ESD stress through interface pins. Design emphasis should be placed on enhancing single-side ESD performance, i.e., the protection capability between interface pins and system ground (I/O to Isolation GND).

(2) Isolation ICs (e.g., isolators, isolated power supplies): ESD impacts at interfaces create significant voltage differences across the isolation barrier. These devices require optimized dual-side ESD performance, i.e. the protection capability for cross-barrier coupling (PE to Isolation GND).

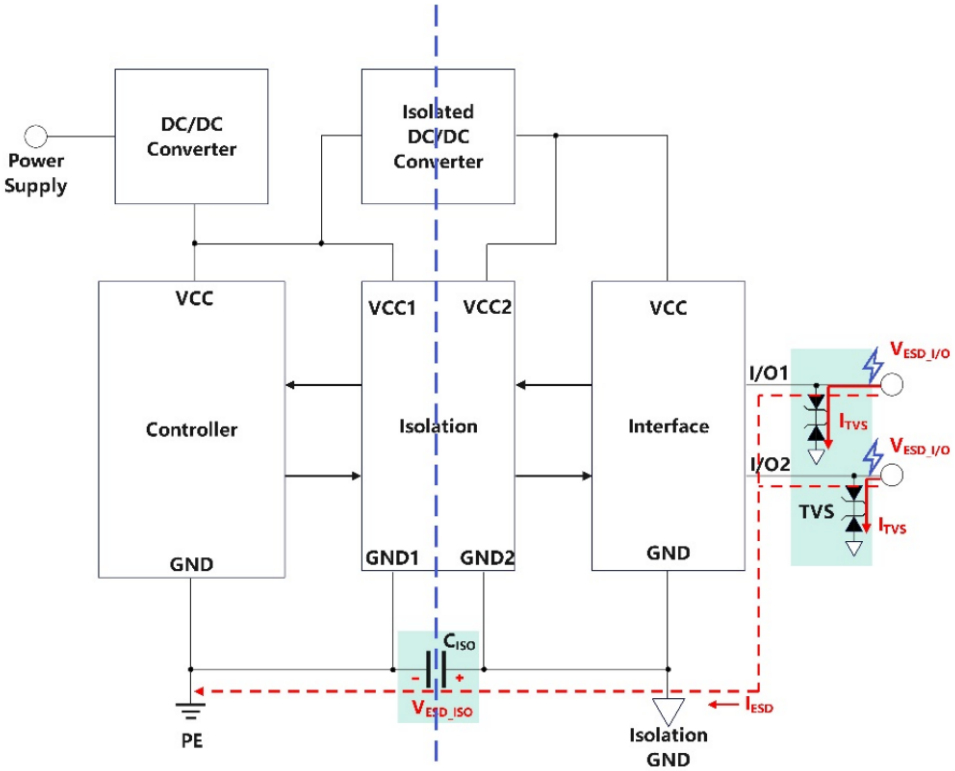


Figure 5.1 ESD Protection Schematic for Isolated Systems

For single-side ESD protection, common methods include adding TVS diodes, peripheral resistors, or ferrite beads. Peripheral resistors and ferrite beads can affect data transmission, whereas TVS diodes with low capacitance characteristics are preferred for high-speed data transmission. When the circuit operates normally, the TVS diode remains in a cut-off (high-impedance) state, which will not affect normal operation. When transient voltage spikes reach the breakdown voltage of the TVS, it rapidly switches to a low-impedance state, discharging transient currents to ground and clamping abnormal voltages to lower levels, thereby protecting subsequent circuits from overvoltage damage.

For dual-side ESD protection, TVS conduction creates open-circuit voltage stress from the ESD pulse on the secondary-side isolation GND, generating high-voltage stress across the isolation barrier. The components bearing such high voltage stress are the equivalent parasitic capacitances C_{ISO} of the isolation barrier, composed of isolator gate capacitance, PCB pin-to-pin capacitance, and PCB primary-secondary parasitic capacitance. Parallel safety capacitors (Y capacitors) on the primary and secondary sides increase C_{ISO} values, filtering out high-voltage narrow pulses and thus effectively enhancing dual-side ESD capability.

Additionally, during system-level ESD testing, any potential air discharge phenomena should be avoided, such as inter-pad discharges, discharges from conformal coating on components, discharges from pin tips of through-hole components, discharges from plane copper edges on PCB primary and secondary grounds, and enclosure coupling discharges. This ensures the richness of injected ESD pulses and improves the reproducibility of ESD tests.

4.Revision History

Revision	Description	Author	Date
1.0	Application Note created	Shuo Zhang, Runsheng Zhou, Minqi Zhao	2025/2/16